PATENT

2184
#5
BT
3-14-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Douglas E. Duschatko, Andrew J. Thurston		
Assignee:	CISCO TECHNOLOGY, INC.		
Title:	ERROR INSERTION CIRCUIT FOR SONET FORWARD ERROR CORRECTION		
Serial No.:	09/821,948	Filing Date:	March 30, 2001
Examiner:	Unknown	Group Art Unit:	2184
Docket No.:	CIS0071US		

Austin, Texas
February 27, 2003

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT
37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying PTO Form-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made; or

3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on February 27, 2003.

Attorney for Applicant(s) — Date of Signature: 2/27/03

Respectfully submitted,

Marc R. Ascolese
Attorney for Applicant(s)
Reg. No. 42,268
512-439-5085
512-439-5099 (fax)